**IN THE DRAWINGS:**

Drawing sheet 1, which includes FIG. 1, has been amended and replaced by a replacement sheet. The amendment includes adding references designators for specific signal names described in the specification. No new matter has been added.

## REMARKS

Claims 1-23 were pending in the present application. Claim 17 was amended to fix a typographic error. Accordingly, claims 1-23 remain pending in the present application.

The drawings were objected to by the Examiner. The drawings and the specification have been amended to overcome the Examiner's objections. A replacement sheet including amended FIG. 1 is attached herewith.

However, with respect to the Examiner's objection in regard to FIG. 4, Applicant respectfully submits FIG. 4 is a pin assignment table showing pin numbers and pin names. Therefore, the exemplary pin numbers and pin names shown in FIG. 4 are not a reference characters as the term is used in 37 C.F.R. 1.84 (p)(5). Accordingly, Applicant submits FIG. 4 and its corresponding description fulfils the requirements of37 C.F.R. 1.84 (p)(5).

Claims 1-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Endo et al. (U.S. Patent Number 5,535,169) (hereinafter "Endo") in view of Stevens et al. (U.S. Patent Number 6,636,957) (hereinafter "Stevens"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites

> "A memory module comprising:
>
> a plurality of memory devices;
>
> a control circuit configured to generate **a** chip select signal that is provided to **each** of said plurality of memory devices, wherein said chip select signal is dependent upon assertions of a **first** bank chip select signal **and** a **second** bank chip select signal;

wherein said control circuit is further configured to generate an address signal that is provided to each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted." (Emphasis added)

The Examiner asserts Endo teaches nearly all the limitations of Applicant's claim 1. The Examiner acknowledges Endo does not teach or disclose the memory module or the serial presence detect. The Examiner further asserts Steven's teaches a memory module including the serial presence detect. Applicant respectfully disagrees with the Examiner's characterization of Endo and with the Examiner's assertion that the combination of Endo and Steven's teaches the combination of features recited in Applicant's claim 1.

Specifically, Endo is directed to a semiconductor memory device (e.g., SDRAM chip) in which Endo teaches generating an internal refresh signal from a chip select signal, which may overcome conventional refresh techniques. More particularly, Endo teaches

> "A semiconductor memory device includes a plurality of banks each having a memory cell array and sense amplifiers, a data input/output circuit and an address circuit. A first part of the device receives control signals from an outside of the semiconductor memory device and generates a refresh signal therefrom." (*See* Abstract)

Endo also teaches at col. 4, lines 27-

> "A refresh signal generating circuit 30 receives control signals supplied from the outside of the circuit 30, and generates a refresh signal therefrom. In the example shown in FIG. 3, the refresh signal generating circuit 30 generates the refresh signal REFR from **the** chip select signal /CS, the row address strobe signal /RAS and the column address strobe signal /CAS. The control signals from the outside of the circuit 30 are generated one time with respect to one access operation in which a plurality of banks (four banks #0-#3 in the refresh operation are sequentially accessed one time. In the aforementioned prior art, there is a need to generate the control signals four times in order to access four banks #0-#3.
> An automatic bank select signal generating circuit 32 receives the above refresh signal REFR, and automatically outputs bank select signals BS0-BS3 used to sequentially select four banks #0-#3 one by one. A latch enable signal generating circuit 34 generates, from the refresh signal REFR and the bank select signals BS0-BS3, latch enable signals LE0-LE3

used to activate sense amplifiers provided in banks #0-#3." (Emphasis added)

From the forgoing description, it is clear to Applicant Endo teaches a memory device such as an SDRAM chip that uses a single chip select signal, received from outside the chip, to generate a refresh signal within the chip. The internal refresh signal is then used to generate bank select signals within the chip for refresh operations. Endo does not use any language to suggest receiving more than one chip select signal. Nor does Endo discuss generating a single chip select from the two chip selects. In addition, Endo does not mention generating an address signal dependent upon the two received chip select signals.

Stevens is directed toward initializing memory devices on memory modules using a serial interface.

Applicant respectfully submits that the Examiner has used a piecewise application of Endo and Stevens when combining the references. Applicant submits that just because Stevens teaches a memory module, there is no motivation to combine the references, either explicitly or inherently in either reference. Furthermore, Applicant submits irrespective of the fact that Endo does not teach the limitations recited in Applicant's claims, the techniques taught by Endo are not even generally applicable to a memory module as a whole, nor does Endo seek to solve a problem even remotely similar to Applicant's problem.

Thus, Applicant submits neither Endo nor Stevens taken either singly or in combination, teach or suggest the combination of features taught in Applicant's claim 1. Specifically, neither Endo nor Stevens teach or suggest a memory module comprising "a control circuit configured to generate **a** chip select signal that is provided to **each** of said plurality of memory devices, wherein said chip select signal is dependent upon assertions of a **first** bank chip select signal **and** a **second** bank chip select signal," as recited in Applicant's claim 1. In addition, neither Endo nor Stevens teach or suggest "wherein said control circuit is further configured to generate an address signal that is provided to

each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said **first** bank chip select signal and said **second** bank chip select signal are asserted," as recited in Applicant's claim 1.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Endo in view of Stevens for the reasons given above.

Applicant's claim 15 recites features that are similar to features recited in claim 1. Thus, Applicant believes claim 15, along with its dependent claims, patentably distinguishes over the cited art for at least the reasons given above.

Applicant's claim 18 recites

> "A method of emulating a two rank memory module using a single rank memory module, said method comprising:
>
> receiving a **first** bank chip select signal and a **second** bank chip select signal on said single rank memory module;
>
> generating a chip select signal and providing said chip select to each of a plurality of memory devices mounted to said single rank memory module, wherein said chip select signal is dependent upon assertions of said **first** bank chip select signal and said **second** bank chip select signal;
>
> generating an address signal and providing said address signal to each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted." (Emphasis added)

As described above neither Endo nor Stevens taken either singly or in combination, teach or suggest the combination of features taught in Applicant's claim 18. Thus, Applicant submits claim 18 patentably distinguishes over Endo in view of Stevens for the reasons given above.

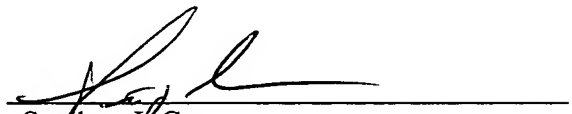
Applicant's claim 21 recites features that are similar to features recited in claim 18. Thus, Applicant believes claim 21, along with its dependent claims, patentably distinguishes over the cited art for at least the reasons given above.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-69100/SJC.

Respectfully submitted,



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